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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,009	12/31/2001	Zhi-Hao Lin	26870-4	7508

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EXAMINER	
SHIFERAW, ELENI A	
ART UNIT	**PAPER NUMBER**
2136	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,009	LIN, ZHI-HAO	
	Examiner	Art Unit	
	Eleni A. Shiferaw	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments/amendments with respect to amended claims 1, 10, and 21, presently pending claims 1-21, filed on June 24, 2005 have been fully considered but they are not persuasive. The examiner would like to point out that this action is made final (MPEP 706.07a).

2. The examiner accepts the amended claim 11.

3. The examiner withdraws the objection made to claim 21, under 37CFR 1.75, as being a substantial duplicate.

Response to Arguments

4. Applicant argues that:

a. Independent claims 1 and 21 are not taught by either references, whether alone or in combination, to include *"executing a protection action...," "operating said product characteristic value..." and "comparing said operation value..." and "the network environment disclosed by Veil teaches away from the standalone computer environment of the claimed invention"* (page 8 par. 3).

b. The references, whether alone or in combination, fail to support *"the protection action for a specific one of a program area and data area when the* ***at least one product*** *does not have a characteristic value conforming to usage standards of a specific one of the program area and data area"* (page 9 par. 1).

c. Dependent claims 2-20 are allowable based upon their dependency on allowable claim 1.

However, Examiner disagrees with applicant.

Regarding argument (a), Argument is not persuasive. Veil and Cromer teaches all the claimed limitations as claimed on the Office Action. Veil teaches determining whether new peripherals have been added to the system and validating any new secured peripherals (col. 10 lines 8-12) by reading and verifying the products/peripherals/second computer serial number (Veil Fig. 4 No. 204 & 212, and col. 9 lines 16-25 and lines 47-67) and operating said product characteristic value through an algorithm to obtain an operation value or hash algorithm is used to obtain hash output result for product verification (Veil Col. 9 lines 47-67; hash algorithm) and the hash output is compared to verify if the product is new (Veil Col. 9 lines 47-col. 10 lines 20). Applicant also argues Veil's network environment teaches away from standalone computer. However applicant did not claim standalone computer nowhere in the claims 1 and 21, **but product**. Product is n-secure peripherals in Veil's invention. However the Office also rejected applicant's claimed limitation "...product...", as a computer peripherals like processor, memory, hard drive, and etc, **in light of the specification** (first Office Action page 4-5).

Regarding argument (b), Argument is not persuasive. Veil teaches the protection action for a specific one of a program area and data area when the **at least one product** does not have a characteristic value conforming to usage standards of a specific one of the

program area and data area (Veil Col. 10 lines 39-44, executing a protection action, not executing application, when the peripherals are not known or not listed on the BIOS memory).

Regarding argument (c), examiner disagrees with applicant. Based on the arguments set forth by the examiner for arguments (a) and (b), the dependent claims stand rejected.

The examiner is not trying to teach the invention but is merely trying to interpret the claim language in its broadest and reasonable meaning. Therefore, the examiner asserts that the system of the prior art, Veil and Cromer teach or suggest the subject matter as recited in independent claims 1 and 21. Dependent claims 2-20 are also rejected at least by virtue of their dependency on independent claims and by other reason set forth in this office action dated September 9, 2005 Accordingly, rejections for claims 1-21 are respectfully maintained.

Rejections

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

6. Claims 1-3 and 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Veil (Patent Number: 6,138,239) in view of Cromer et al. (Cromer Pub. No. US 2003/0084278 A1).

As per claims 1 and 21, Veil teaches a method for protecting a specific one of a program area and a dada area having specific usage standards to be applied to a basic input/output system (BIOS), wherein said basic input/output system defines a mapping table therein, said method comprising steps of:

providing at least one product (peripherals) and reading a product characteristic value of said at least one product (Veil Fig. 4 No. 204 & 212, and col. 9 lines 16-25 and lines 47-67; providing a first and second peripherals and reading the first and second peripherals, serial numbers, to be validated/authenticated by BIOS);

operating said product characteristic value through an algorithm to obtain an operation value (Veil Col. 9 lines 47-67; hash algorithm);

comparing said operation value (hash output) with said mapping table to decide whether said at least one product has said characteristic value conforming to said usage standards of said specific one of said program area and said data area (Veil Col. 9 lines 47-col. 10 lines 20, and Fig. 2C No. 142; BIOS determines/verifies if the peripherals are new/secure by comparing the hash output); and

executing a protection action (application is not executed) for said specific one of said program area and said data area when said at least one product does not have said characteristic value conforming to said usage standards of said specific one of said program area and said data

area, thereby preventing said specific one of said program area and said data area from being misappropriated illegally (Veil Col. 10 lines 39-44; executing a protection action, not executing application, when the peripherals are not known or not listed on the BIOS memory).

Veil fails to explicitly teach the products as applicant's specification;

However Cromer teaches plurality of devices/peripherals like processor, memory, floppy drive, and hard drive are coupled to BIOS. Cromer BIOS determines if the devices are bootable or not bootable and BIOS lists devices in a boot table, and then initiate a boot sequence or generate an interrupt signal depending on the determination result in using hash algorithm (Comer Page 1 par. 0006-0007 and page 2 par. 0019-0020).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to employ the teachings of Cromer within Veil because it would allow to determine bootable or non-bootable peripherals/devices for BIOS initialization or boot up by reading the products ID/serial number value, and operating the product ID value through a hash algorithm, and comparing the hash value result in order to determine if the hash value result matches the pre-registered/predetermined code/data stored in BIOS. If unauthorized code is present in the devices/peripherals, the digest value resulting from a hash of that code will produce a value that differs from predetermined value and the operating system take appropriate action/protection action (Cromer Page 1 par. 0006-0008, and page 2 par. 0022).

As per claim 2, both Veil and Cromer teach all the subject matter as described above. In addition,

a method wherein said product characteristic value is obtained via reading contents of said at least one product (Veil Fig. 4 No. 204 & 212, and col. 9 lines 16-25 and lines 47-67; providing a first and second peripherals and reading the first and second peripherals, serial numbers, to be validated/authenticated by BIOS, and Cromer Fig. 2B No. 122).

As per claim 3, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said at least one product is selected from a group consisting of a system chipset, a PCI/ISA card, a ROM, a CMOS, a CPU, a computer peripheral device, and the combination thereof (Veil Fig. 4 No. 204 & 212, and Cromer Fig. 1 No. 20, 70, 50, 60, and 40; peripherals).

As per claim 13, both Veil and Cromer teach all the subject matter as described above. In addition, Veil discloses a method wherein said algorithm is a secret code algorithm (Veil Col. 9 lines 55-67).

As per claim 14, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said secret code algorithm is one of a summing algorithm and an operating function algorithm (Veil Col. 9 lines 55-67).

As per claim 15, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said protecting action is to skip said specific one of said program

area and said data area (Veil Col. 10 lines 39-44 and Cromer page 1 par. 0007 and page 2 par. 0020). The rational for combing are the same as claim 1 above.

As per claim 16, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said protecting action is to shutdown the operating system (Veil Col. 10 lines 39-44, and Cromer page 1 par. 0007 and page 2 par. 0020). The rational for combing are the same as claim 1 above.

As per claim 17, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said protecting action is to halt the operating system (Veil Col. 10 lines 39-44, and Cromer page 1 par. 0007 and page 2 par. 0020). The rational for combing are the same as claim 1 above.

As per claim 18, both Veil and Cromer teach all the subject matter as described above. In addition, a method wherein said protecting action is to produce a flag signal to be stored in a storage device for protecting said specific one of said specific program area and data area (Veil Col. 10 lines 39-44, and Cromer page 1 par. 0007 and page 2 par. 0020). The rational for combing are the same as claim 1 above.

As per claim 19, both Veil and Cromer teach all the subject matter as described above. In addition, method wherein said program area and said data area are stored in a storage module (Veil Col. 10 lines 39-44, and Cromer Page 2 par. 0023).

As per claim 20, both Veil and Cromer teach all the subject matter as described above. In addition, method wherein said operation value is one of a specific value and a supplemental value (Veil Col. 9 lines 56-59).

7. Claims 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Veil (Patent Number: 6,138,239) in view of Cromer et al. (Cromer Pub. No. US 2003/0084278 A1) and further in view of Cepulis et al. (Cepulis, Patent No.: US 6,463,550 B1).

As per claim 4, both Veil and Cromer teach all the subject matter as described above.

Veil and Cromer fail to teach a clock generator, a South Bridge chipset, a North Bridge chipset, a Communication chipset, a Super I/O chipset, a Video Graphics Array chipset, a small computer system interface chipset, a Local Area network chipset, a sensor chipset, a health chipset, a PCI/PCI Bridge chipset, an IDE ATA Controller chipset, a PCI/ISA Bridge chipset, a 1394 chipset, and the combination thereof.

However Cepulis discloses method wherein said system chipset is selected from a group consisting of a clock generator, a South Bridge chipset, a North Bridge chipset, a Communication chipset, a Super I/O chipset, a Video Graphics Array chipset, a small computer system interface chipset, a Local Area network chipset, a sensor chipset, a health chipset, a PCI/PCI Bridge chipset, an IDE ATA Controller chipset, a PCI/ISA Bridge chipset, a 1394 chipset, and the combination thereof (Cepulis Col. 1 lines 27-42, and col. 8 lines 39-42).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the teachings of Cepulis within the combination system of Veil and Cromer because it would protect different kinds of chipset programs from being copied by an authorized person.

As per claim 5, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein said PCI/ISA card is selected from a group consisting of a sound card, a TV card, a VGA card, a SCSI card, a LAN card, an IDE card, an AMR card, a CNR card, a Modem card, and the combination thereof (Cepulis Col. 8 lines 36-43). The rational for combining are the same as claim 4 above.

As per claim 6, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein said ROM is selected from a group consisting of an EEPROM, an EPROM, a PROM, a ROM, a Flash Memory, and the combination thereof (Cepulis Col. 7 lines 66-col. 8 lines 6). The rational for combining are the same as claim 4 above.

As per claim 7, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein the product characteristic value of said ROM is based on one data selected from a group consisting of a Checksum value, a Class code, a Sub-class code, a Revision ID, a Device ID, a Vendor ID, a Manufacturer ID, a Product ID, a Sub-Product ID, a Sub-Device ID, a Sub-Vendor ID, a ROM Signature, a Data Structure Length, a

Data Structure Revision, an Image Length, a Revision Level of Code/Data, a code Type, a Command Code, a Control Register, a Status Register, an Expansion ROM Base Address, a Configuration type, a Serial Presence Detect Data, a Clockgen device related data, and a specific address data (Cepulis Col. 7 lines 66-col. 8 lines 6). The rational for combining are the same as claim 4 above.

As per claim 8, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein said CMOS is used for storing a relevant set value of said BIOS (Cepulis Fig. 1 No. 122). The rational for combining are the same as claim 4 above.

As per claim 9, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein said product characteristic value is selected from a group consisting of an ID, a Patch ID, a relevant register value of said CPU, and combination thereof (Cepulis Fig. 2 No. 104). The rational for combining are the same as claim 4 above.

As per claim 10, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, Cepulis discloses a method wherein said computer peripheral device is selected from a group consisting of a Modem, a Printer, a Serial Port Device, a Parallel port device, a SCSI Device, an IDE Device, a UBS Device, a midi Device, and the combination thereof (Cepulis Col. 1 lines 28-42). The rational for combining are the same as claim 4 above.

As per claim 11, Veil, Cromer, and Cepulis teach all the subject matter as described above. In

addition, Cepulis discloses a method wherein said SCSI Device, said IDE Device, and said Device are provided by a group consisting one of a diskette, a hard disk, a compact disc, a ZIP disk, a LS-120 disk, a type, and the combination thereof (Cepulis Col. 1 lines 28-42). The rational for combining are the same as claim 4 above.

As per claim 12, Veil, Cromer, and Cepulis teach all the subject matter as described above. In addition, a method wherein said product characteristic value is one selected from a group consisting of a register value, an I/O port value and the combination thereof in said at least one product (Cromer Fig. 1 No. 40 and page 1 par. 0004 lines 10-12).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eleni A Shiferaw whose telephone number is 571-272-3867. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz R Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eleni Shiferaw
Art Unit 2136
September 9, 2005

AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
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